REMARKS

Claims 1-27 are pending in the application and stand rejected. Claims 1, 2, 7, 8, 10, 11, 16, 17, 20, 21, 25, 26, 27 have been amended. Reconsideration of the rejections is respectfully requested.

Claim Rejections- 35 U.S.C. §102

Claims 1-6, 10-15, 20-21 and 25-27 were rejected as being anticipated by U.S. Patent No. 6,052,330 to Tanabe for the reasons set forth on pages 2-9 of the Office Action. It is respectfully submitted that at the very least, claims 1, 10, 20, 21, 25, 26, 27 are not anticipated by Tanabe. For instance, Tanabe does not disclose or suggest devices and methods for, e.g., *controlling a data width of the data buffer in response to one or more address bits of an external address signal*, as essentially claimed in claims 1, 10, 20, 21, 25, 26, 27.

In particular, on a fundamental level, Tanabe does not disclose or suggest methods for controlling the data width of a data buffer (input buffer or output buffer). Tanabe discloses, for example, methods for masking arbitrary data bits of data that are sequentially (consecutively) read at a higher clock frequency than a clock frequency for a burst operation (see, e.g., Col. 6, lines 65-67).

Indeed, as illustrated in FIGs. 8 and 9 of Tanabe, the methods and devices of Tanabe are adapted for generating control signals for masking arbitrary data of a plurality of consecutive data which are written to memory in response to input data mask control signals (DINM1 and DINM2) (see FIG. 9) and for masking arbitrary data of a plurality of consecutive data which are read from memory in response to an output data mask control signal (DOUTM) (see FIG. 8), as described in, e.g., Col. 12, lines 40-51).

In this regard, Tanabe clearly does not disclose or suggest devices and methods for controlling the data width of a data buffer as contemplated by the claimed inventions to provide

variable data I/O widths, e.g., X8, X6, X4, X2, for memory access operations (see, e.g., FIGs. 5 and 6 of Applicants' Specification) in which blocks or words of n-bit data are concurrently read from/written to memory. .

Furthermore, Tanabe clearly does not disclose or suggest using *one or more address bits of an external address signal* for data width control. Indeed, Tanabe discloses in FIG. 1 the use of separate control signal pins for inputting a plurality of input-output data mask control signals DQM1 and DQM2, which are processed by a data mask control circuit to generate the data mask control signals DOUTM and DINM1 and DINM2. These signals DQM1 and DQM2 are independent from the address bits of external address signals applied on the address bus AB (see, Col. 2, lines 33-38). In this regard, the data mask control circuit (7) clearly does not decode or otherwise process one or more address bits of an external address signal, as contemplated by the claimed inventions.

Therefore, for at least the above reasons, claims 1, 10, 20, 21, 25, 26, 27 are patentably distinct and patentable over Tanabe. Moreover, claims 2-6 and 11-15 are patentably distinct and patentable over Tanabe at least by virtue of their dependence from respective base claims 1 or 10. Accordingly, withdrawal of the anticipation rejections is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 7-9 and 16-19 stand rejected as being unpatentable over Tanabe in view of U.S. Patent No. 4,706,219 to Miyata. Claims 22-24 stand rejected as being unpatentable over Tanabe in view of U.S. Patent No. 5,349,448 to Hirai.

These obviousness rejections are based, in part, on the primary reference Tanabe as anticipating claims 1, 10 and 20. In this regard, it is respectfully submitted that the cited combinations of references are legally deficient to establish a *prima facie* case of obviousness

against claims 7-9, 16-19 and 22-24 for *at least* the same reasons given above for claims 1, 10 and 20. Moreover, the references Miyata and Hirai clearly do not cure the deficiencies of Tanabe as noted above with regard to claims 1, 10 and 20. Accordingly, the withdrawal of the obviousness rejections is respectfully requested.

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